REMARKS

In the Office Action, claims 1-3 and 5-10 were rejected under 35 U.S.C. § 112, second paragraph. Claims 1-3 and 5-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over USP 6,316,838 issued to Ozawa et al. (hereinafter "Ozawa"). Claims 11-13 and 15-20 were also rejected under 35 U.S.C. § 103(a) as being unpatentable over USP 5,822,214 issued to Rostoker et al. (hereinafter "Rostoker") alone or in combination with Ozawa. In this Amendment, Applicants have only amended claim 1. Accordingly, claims 1-3, 5-13 and 15-20 will be pending after entry of this Amendment.

I. Rejection of Claims Under 35 U.S.C. § 112, Second Paragraph

In the Office Action, the Examiner rejected claims 1-3 and 5-10 under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Specifically, the Examiner stated that the phrase "said conductors" in claim 1, line 7 was not clearly defined. Applicants have amended claim 1 to clarify the referent for the phrase and respectfully contend that the amendment has overcome the Examiner's rejection.

II. Rejection of Claims Under 35 U.S.C. § 103(a)

A. Patentability of Claims Over Ozawa

In the Office Action dated 04/03/2003, the Examiner found claims 1-3 and 5-10 to be unpatentable over Ozawa. The Examiner stated that Ozawa "discloses an integrated circuit" comprising, among other elements, horizontal and diagonal conductors. Applicants respectfully disagree with the Examiner's finding and traverse the rejection with arguments presented below.

i. An Integrated Circuit Is Different than a Protective Package Containing an Integrated Circuit

The subject application provides a definition of "Integrated Circuit" in its first substantive paragraph:

> An integrated circuit ("IC") is a semiconductor device that includes many electronic components (e.g., transistors, resistors, diodes, etc.). These components are often interconnected to form multiple circuit components (e.g., gates, cells, memory units, arithmetic units, controllers, decoders, etc.) on the IC. The electronic and circuit components of ICs are jointly referred to below as "components". An integrated circuit also includes multiple layers of metal and/or polysilicon wiring that interconnect its electronic and circuit components. [Paragraph 0001]

Typically, before an integrated circuit can be used in an electronic product, it must be put in a protective package. The package provides a number of functions with respect to the integrated circuit, including physical protection and the provision of a substantial lead system. An enclosure ensures the physical protection of an integrated circuit. Where the enclosure is a plastic package, the enclosure is typically made from an epoxy resin. A direct connection between the IC and electronic product cannot be made, because the interconnect components of an IC are too thin and fragile. The lead system allows such a connection to be made by providing a more substantial interface (metal leads) between the IC and the electronic product. A copy of Chapter 18 from a book entitled "Microchip Fabrication" has been included with this Response for the Examiner's convenience. The chapter describes package requirements, functionality and construction.

ii. Ozawa Discusses a Package

Ozawa's semiconductor device is a protective package, not an integrated circuit. This is shown through Ozawa's constant reference to package construction techniques.

For instance, Ozawa refers to the encapsulation of semiconductor elements within an epoxy resin 26. [Col. 3, line 66 to Col. 4, line 3 and Col. 4, lines 60-64] The document further describes wire bonding pads (Col. 5, lines 7-17), flip-chip bonding (Col. 4, lines 18-27), and lead connecting pads (Col. 5, lines 38-44).

As described above, epoxy resin encapsulation is a common technique for enclosing an integrated circuit within a plastic package. Wire bonding and flip-chip bonding are techniques used for package production. This is illustrated in reference to Chapter 18 of "Microchip Fabrication":

> The wire bonding procedure is simple in concept. A thin (0.7- to 1.0-mil) wire is first bonded to the chip bonding pad and spanned to the inner lead of the package lead frame. [Page 565]
>
> Flip-chip and bump technology: Wire bonding presents several problems. Minimum height limits are imposed by the required wire loops. There is a chance of electrical performance problems or shorting if the wires come too close to each other. The wire bonds require two bonds and must be placed one-by-one and there are resistances associated with each bond. These problems are addressed by replacing wires with a deposited metal *bump* on each bonding pad. Connection to the package is made when the chip is flipped over and soldered. [Pages 567-568]

As to "lead connection pads," leads are both connected to the integrated circuit through bonding wires and to the electronic product. [See page 559 of "Microchip Fabrication"]

What the Examiner believes to be integrated circuit conductors, therefore, are actually wires within a package between lead connecting pads (L/C pads, Col. 5, lines 41-44) and flip-chip pads (F/C pads, Col. 4, lines 14-17). In other words, Ozawa does not disclose an integrated circuit comprising horizontal and diagonal conductors.

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iii. Applicants Claim an Integrated Circuit

Applicants claims are directed to an integrated circuit and are accordingly distinguished from Ozawa's package.

iv. The Rejection Over Ozawa Should Be Withdrawn

Given that Ozawa reports a package rather than an integrated circuit, the reference clearly does not teach, suggest or motivate one ordinary skill to produce Applicants' integrated circuit. Respectfully, the rejection under 35 U.S.C. § 103(a) should be withdrawn.

B. Patentability of Claims in View of Rostoker

In the Office Action dated 04/03/2003, the Examiner found claims 11-13 and 15-20 to be unpatentable over Rostoker. The Examiner stated, among other things, that Rostoker discloses the following:

> a plurality of metal layers 117-119 with each metal layer comprising a plurality of conductors to interconnect points on the integrated circuit, at least fifty (50) percent of the conductors on a first metal layer 119 being deposed in a first preferred diagonal direction. . . .(See figures 4 and column 14, lines 1-14) [Office Action Page 6]

Applicants respectfully disagree with the Examiner's finding and traverse the rejection with arguments presented below.

i. The Sections of Rostoker Cited by the Examiner Do Not Disclose a Plurality of Diagonal Conductors Deposed in a Preferred Direction

First, col. 14, lines 1-14 clearly does not disclose a plurality of metal layers where at least 50 percent of the conductors are deposed in a preferred diagonal direction. This is seen through simple reference to the text:

> A conventional rectangular routing arrangement is illustrated. The first metal layer 100 provides for electrical connections in a direction that is angularly displaced 90 degrees from electrical connections provided by the second metal layer 101. For example, in the M1 layer 100, a point 103 is connected to a point 104 by a metal wire 105. In the M2 layer 101, a point 106 is connected to a point 107 by a metal wire 108. The wire 105 is angularly displaced 90 degrees from the wire 108; in other words, the wire 105 in M1 layer 100 is perpendicular to wire 108 in the M2 layer 101. Wires in the same layer will be parallel to each other. For example, point 109 in the M1 layer 100 is connected to point 110 by a wire 111. The wire 111 is parallel to the wire 105 in the same M1 metal layer 100, and is perpendicular to the wire 108 in the M2 metal layer 101. [Col. 13, line 67 to Col. 14, line 14, emphasis added]

The text plainly states that "conventional rectangular routing" is illustrated, not diagonal routing.

Second, a review of Figure 4 reveals that layer 119 shows one purportedly diagonal line; layer 118 shows one purportedly diagonal line; and, layer 117 shows two purportedly horizontal lines. One line is not a "plurality," which means a "plurality" of diagonal lines is not shown in any layer of Figure 4. Therefore, in contrast to the Examiner's finding, Rostoker does not disclose a plurality of metal layers where at least 50 percent of the conductors are deposed in a preferred diagonal direction.

ii. Rostoker Accordingly Does Not Teach, Suggest or Provide Motivation to One of Ordinary Skill in the Art to Arrive at Applicants' Invention

Given that Rostoker does not disclose the diagonal conductors of Applicants' invention, one of ordinary skill certainly would not be motivated to first construct layers of such conductors and then to incorporate at least one zag conductor. [See claim 11] That magnitude of conceptual leap cannot properly be characterized as an obvious one. Applicants accordingly contend that the rejection under 35 U.S.C. § 103(a) over Rostoker should be withdrawn.

iii. Rostoker and Ozawa Cannot Be Combined to Arrive at Applicants' Invention

As shown above, Ozawa is directed to a protective package, not an integrated circuit. Its combination with Rostoker would not provide Applicants' integrated circuit. Applicants respectfully submit, therefore, that the 35 U.S.C. § 103(a) rejection over Rostoker in view of Ozawa should be withdrawn.

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CONCLUSION

In view of the foregoing, it is submitted that the claims are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

Respectfully submitted,

Dated: September 3, 2003

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Chapter

18

Packaging

Overview

After wafer sort, the chips on the wafer surface are completed and the electrically functioning ones are identified. The chips will be incorporated into an individual protective package, mounted with other components in hybrid or multichip modules, or connected directly onto a printed circuit board. This chapter will describe the packages and processes used for chip protection.

Objectives

Upon completion of this chapter, you should be able to:

1. List the four functions of a semiconductor package.
2. List the five common parts of a package.
3. Recognize and identify the major package designs.
4. List and describe the major packaging process flows.

Introduction

After wafer sort, the chips are still part of the wafer. For use in a circuit or electronic product they must be separated from the wafer and, in most cases, put in a protective package. They may also be mounted onto the surface of a ceramic substrate as part of a hybrid circuit, put into a large package with other chips as part of a multichip module (MCM) or connected directly onto a printed-circuit board (Fig. 18.1).

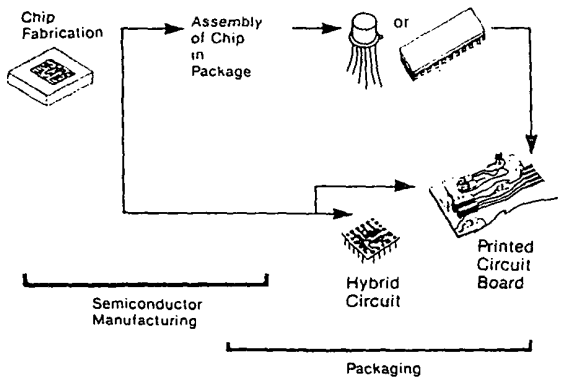

Figure 18.1 Chip packaging options.

All three options share some common processes. In this chapter, the basic packaging processes and the types of packages used to protect the chip will be explained. This series of processes is known variously as *packaging, assembly,* or the *back-end process.* In the packaging process, the chips are called *dies* or *dice* and in certain parts of the country they are referred to by the Texas Instruments' term, *bars.* In this chapter they will be referred to as *chips* or *die.*

Over the years, semiconductor packaging has lagged behind wafer fabrication in process sophistication and manufacturing demands. The advent of the VLSI–ULSI era in chip density has forced a radical upgrading of chip packaging technology and production automation. Higher-density chips result in more bonding pads, requiring more electrical connections and cleaner packages and processes. The SIA technology roadmap is projecting packages with up to 1000 chip connections to package very large memory chips. As solid-state circuits have found more applications, the need for special package designs has increased. The chips may end up in either consumer products or the demanding and harsh environments of space, automotive, and military hardware. These harsh environments require special packaging, processing, and testing to ensure high reliability in the field. These packages, processes, and tests are referred to as *hi-rel* (high-reliability). The other chips and packages are referred to as *commercial* parts.

No longer is packaging the stepchild of the semiconductor industry. Many feel that eventually packaging will be the limiting factor on the growth of chip size. For the time being, however, much effort is going into new package designs, new material development, and faster and more reliable packaging processes.

Chip Characteristics

Throughout this text many characteristics of discrete devices and integrated circuits have been mentioned. Several of them have a direct bearing on package design and the packaging processes (Fig. 18.2). The chip density (integration level) determines the number of connections required, with higher-density chips having larger surface areas and more bonding pads. The trend to larger chips has resulted in the need for thicker and larger-diameter wafers. These factors have caused changes in die separation processes and package design and have created the need for wafer thinning.

In previous chapters it was pointed out that the functioning of the chip components (transistors, diodes, capacitors, resistors, and fuses) can be altered by various contaminants. Primary among them are chemicals such as sodium and chlorine. Additionally, other chemicals can attack the chip layers, and environmental factors, such as particulates, humidity, and static can ruin chips or change their performance. Other concerns are the influence of light and radiation impinging on the chip surface. Some chips are extremely light or radiation sensitive. This factor is considered in the selection of package materials and processing. A dominant chip characteristic is the extreme vulnerability of its surface to physical abuse. The surface components are only a small distance down into the wafer surface, and the surface wiring can be as thin as 1 μm.

These environmental and physical concerns are addressed in two ways. First is the passivation layer deposited near the end of the fabrication process. This layer is known by several different names as listed in Fig. 18.3. The two materials used for the passivation layer are silicon dioxide and silicon nitride. Often they are doped with boron, phosphorus, or both to increase their protective properties. The second method of protecting the chip is provided by a package.

Another chip characteristic of importance to the packaging process is heat generation. Chips used in high-power circuits and

- Integration Level
- Wafer Thickness
- Dimensions
- Environmental Sensitivity
- Physical Vulnerability
- Heat Generation
- Heat Sensitivity

Figure 18.2 Chip characterizations affecting packaging process.

- Silox
- Vapox
- Pyrox
- Glassivation Layer
- PSG
- BSG
- PBSG

Figure 18.3 Passivation layer names.

highly integrated circuits can generate enough heat to actually damage themselves and the circuit. Package design includes heat dissipation factors. Heat is also an important parameter in packaging processes, with packaging process temperatures limited to 450°C. Above this temperature the aluminum and silicon contacts on the chip can form an alloy in the wafer surface that causes electrical shorts.

Package Functions

There are four basic functions performed by a semiconductor package. They are

1. A substantial lead system
2. Physical protection
3. Environmental protection
4. Heat dissipation

Substantial lead system

The primary function of the package is to allow connection of the chip to a circuit board or directly to an electronic product. This connection cannot be made directly due to the thin and fragile metal system used to interconnect the components on the chip surface. The metal leads are typically less than 1.5 μm thick and often only 1 μm wide. The thinnest wires available are 0.7 to 1.0 mils in diameter, which is many times larger than the surface wiring. This difference in wiring sizes is the reason that the chip wiring terminates in the larger bonding pads around the edge of the chip.

Even though the wires are larger, at 1 mil in diameter they too are very fragile. This fragility is overcome by a more substantial electrical lead system that serves as the connection of the chip to the outside world (Fig. 18.4). The lead system is an integral part of the package.

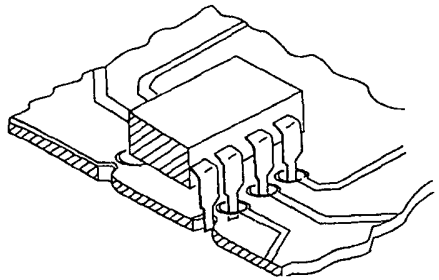

Figure 18.4 Dip through-hole assembly.

Physical protection

The second function of the package is the physical protection of the chip from breakage, particulate contamination, and abuse. Physical protection needs vary from low, as in the case of consumer products, to very stringent, as in the case of automobile circuits, space rockets, and military uses. The protection function is accomplished by securing the chip to a die-attachment area and surrounding the chip, wire bonds, and inner package leads with an appropriate enclosure. The size and eventual use of the chip dictate the choice of materials for the enclosure and the design and size of the package.

Environmental protection

Environmental protection of the chip from chemicals, moisture, and gases that may interfere with the chip functioning is provided by the package enclosure.

Heat dissipation

Every semiconductor chip generates some heat during operation. Some generate large quantities. The package enclosure materials serve to draw the heat away from most chips. Indeed, one of the factors in choosing a package material is its thermal dissipation property. The chips that generate large quantities of heat require additional consideration in the package design. This consideration will influence the size of the package and will often require the addition of metal heat-dissipating fins or blocks on the package.

Packaging Operations

In this section a simple overview of the primary packaging process is presented.

Cleanliness and static control

The vulnerability of the chips to contamination exists during their entire lifetime. While assembly areas are not generally required to maintain the same cleanliness levels as fabrication areas (see Chap. 4), cleanliness is important. The table in Fig. 18.5 lists the common contamination control practices used in packaging areas. Hi-rel areas, particularly, demand higher cleanliness levels. In fact, many companies are finding that half-way contamination control programs are doomed to failure. Consequently, more assembly areas are practicing very stringent controls, especially for people-generated particles and chemicals.

An environmental danger that is most serious in packaging areas is static. In the fabrication clean rooms, static is controlled primarily to prevent the attraction of particles to the wafer surface. This is also a concern in a packaging area. But the greatest concern is *electrostatic discharge,* or *ESD.* Static charge can build up to levels of tens of thousands of volts. If this voltage is suddenly discharged onto a chip surface, it can easily destroy a portion of the circuit. MOS gate structures are particularly vulnerable to ESD.

Every packaging area making high-density chips should have an active antistatic program (Fig. 18.6). Those assembling military parts

- HEPA Filters/VLF Air
- Smocks, Hats, Shoe Covers
- Finger Cots or Gloves
- Filtered Chemicals
- Sticky Floor Mats
- Static Control

Figure 18.5 Contamination control practices.

- Wrist Ground Straps
- Nonstatic Garments
- Antistatic Materials
- Grounded Equipment
- Grounded Work Surfaces
- Grounded Floors or Floor Mats

Figure 18.6 Static control practices.

will need to have one as a condition of getting the contract. The antistatic program is based on operators wearing grounding straps and nonstatic smocks; the use of antistatic carrier materials; moving work by lifting rather than sliding; and grounded equipment, work surfaces, and floor mats. Static is also reduced by the placement of ionizers in nitrogen and air blow-off guns (Fig. 18.7) and in the path of air coming out of HEPA filters.

Basic processes

In wafer fabrication the wafers pass many times in and out of four basic operations (layering, patterning, doping, and heat processing). In packaging also there are several basic operations (Fig. 18.8). However, packaging is a once-through process; each of the major processes is required only once. As in fabrication, the exact order of the operations is determined by the package type and other factors. Each operation may or may not be used in a particular process and each is customized to the particular chip and package requirements.

The basic operations are *backside preparation, die separation, die pick, inspection, die attach, wire bonding, preseal inspection, package*

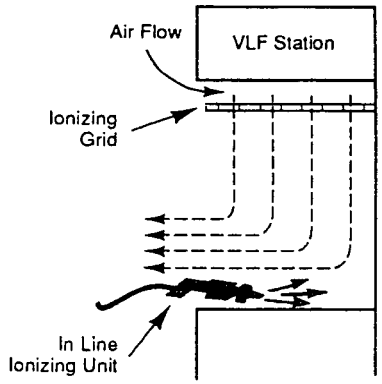

Figure 18.7 Static control techniques.

• Backside Preparation	• Preseal Inspection
• Die Separation	• Packaging Sealing
• Die Pick	• Plating
• Die Attach	• Lead Trim
• Inspection	• Marking
• Bonding	• Final Tests

Figure 18.8 Basic packaging operations.

sealing, plating, trimming, marking, and *final tests.* The details of the various operations and their optional processes are explained in more detail in the remainder of this chapter.

Backside preparation. At the end of the fabrication process some wafers have to be thinned (wafer thinning) to fit in the package and/or to remove backside damage or junctions. Wafers whose die are going to be attached to the package by a gold-silicon eutectic will receive a deposited layer of gold (backside gold).

Die separation. The wafer is separated into individual die by sawing or scribe-and-break techniques.

Die pick and plate. The functioning die identified at wafer sort are picked from the separated wafer and placed in carriers (Fig. 18.9).

Inspection. The plated dies are optically inspected for edge integrity, contamination, and cosmetic defects.

Die attach. Each die is attached into the die-attach area of the package by either a gold-silicon eutectic layer or an epoxy adhesive material (Fig. 18.10).

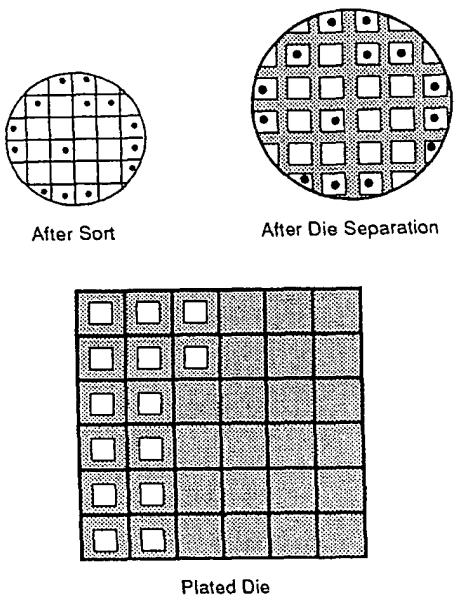

Figure 18.9 Die separation to plate.

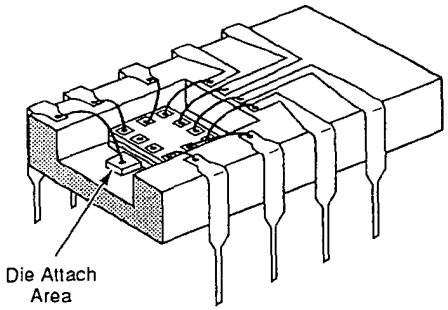

Figure 18.10 Die attach area of package.

Lead bonding. Thin wires are bonded between the chip bonding pads and the inner leads of the package. Bonding is also done by bumps of metal on the bonding pads or by the TAB technique.

Preseal inspection. The bonded die is optically inspected in the package. Criteria checked for are the alignment of the die in the package, proper bond placement, contamination, die-attach quality, and bonding quality.

Plating, trimming, and marking. The outer package leads are plated with an additional layer of conductive metal to improve their solderability into a printed-circuit board. Near the end of the process, each package with outer leads will go through a trimming operation to separate the leads from supports. The marking operation is performed to code important information (Fig. 18.11) on the outside of the package enclosure.

Final test. A series of final tests, including electrical and environmental, are performed on each packaged chip to ensure quality. Some packages will receive a "burn-in" test to detect early failures.

Figure 18.11 Marked package.

Common package parts

The four functions of a chip package are accomplished through the use of a wide variety of package designs. However, most packages have five common parts: the die-attachment area, the inner leads, the outer leads, the chip to package connection, and the enclosure.

Die-attachment area. In the center of every package is an area where the chip is securely attached into the package. This die-attachment area may have an electrical connection that serves to connect the back of the chip to the rest of the lead system. A major requirement for this area is absolute flatness in order to intimately support the chip in the package (Fig. 18.10).

Inner and outer leads. The metal lead system chip is continuous from the die-attach cavity to the printed-circuit board or electronic product. The system inner connections are called the *inner leads, bonding lead tips,* or *bond fingers.* The inner leads are generally the narrowest portion of the lead system. The leads become progressively wider or thicker, finally ending outside the package. These portions of the lead system are called the *outer leads* (Fig. 18.12). Most of the lead systems are composed of one continuous piece of metal. One exception is the side-brazed package. In this package construction method, the outer leads are brazed onto the interior leads. Two different alloys are used for the outer lead system, either an iron-nickel alloy or a copper alloy. The iron-nickel alloy is desirable for its strength and stability, while copper is used for its electrical and heat-conduction properties.

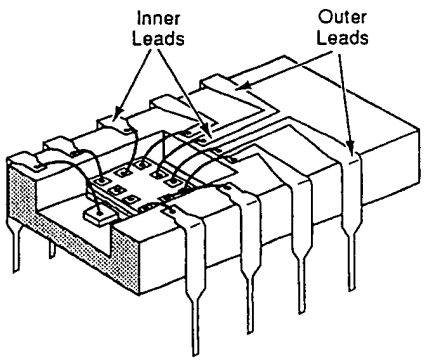

Figure 18.12 Inner and outer leads.

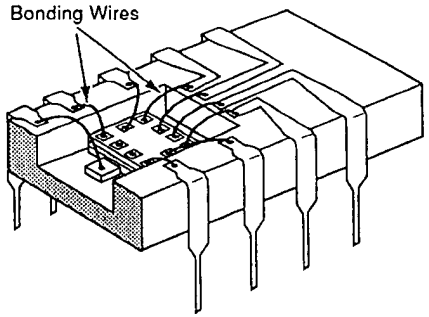

Figure 18.13 Bonding wires.

Chip to package connection

The chip is electrically connected to the lead system of the package with bonding wires, balls, or other on-chip connectors (Fig. 18.13).

Enclosures. The die-attach area and inner and outer leads constitute the electrical parts of the package. The other part is the *enclosure* or *body.* This is the part that provides the protection and heat-dissipation functions. These functions are achieved by several different techniques and package designs as described in the sealing section. The completeness of the seal falls into two categories, hermetic and nonhermetic (Fig. 18.14).

Hermetic sealing results in a package that is impervious to the penetration of moisture and other gases. Hermetic seals are required for chips operating in harsh and demanding environments such as rockets or space satellites. Metal and ceramic enclosures are the preferred materials for hermetically sealed packages.

Nonhermetically sealed packages are adequate for most consumer applications such as computers and entertainment systems. This sealing system provides good and adequate environmental protection of the chip, except in the most demanding situations. A better term

Hermetic
- Metal
- Ceramic

Nonhermetic
- Epoxy Resins
- Polyimides

Figure 18.14 Package sealing designations.

for this type of enclosure sealing method would be "less hermetic." Nonhermetic packages are composed of epoxy resins or polyimide materials and are generally referred to as "plastic packages."

Packaging Processes

Prepackaging wafer preparation

After the final passivation layer and an alloy step in wafer fabrication, the circuits are complete. However, one or two additional processes may be performed on the wafer before transfer to packaging. These steps, wafer thinning and backside gold, are optional, depending on the wafer thickness and the particular circuit design.

Wafer thinning. The trend to thicker wafers presents several problems in the packaging process. Thicker wafers require the more expensive complete saw-through method at die separation. While sawing produces a higher-quality die edge, the process is more expensive in time and consumption of diamond-tipped saws. Thicker die also require deeper die attach cavities, resulting in a more expensive package. Both of these undesirable results are avoided by thinning the wafers before die separation. Another situation requiring wafer thinning is electrical in nature. If the wafer backs are not protected as the wafers go through the dopant operations in fabrication, the dopants will form electrical junctions in the wafer back, which may interfere with good conduction in the back contact, which is required for the circuit to operate correctly. These junctions may require physical removal by wafer thinning.

The thinning step generally takes place between wafer sort and die separation. Wafers are reduced to a thickness of 0.2-0.5 mm.[1] Thinning is done by the same processes (mechanical grinding and chemical-mechanical polishing or CMP) used to grind wafers in the wafer preparation stage (see Chap. 3). An alternate method is to protect the front of the wafers and chemically etch material from the back.

Wafer thinning is a worrisome process. In backgrinding there is the concern of scratching the front of the wafer and of wafer breakage. Since the wafer must be held down on the grinder or polishing surface, the front of the wafer must be protected, and once thinned, wafers break more easily. In backetching there is a similar need to protect the front of the wafer from the etchant. The protection can be provided by spinning a thick layer of photoresist on the front side. Other methods include attaching adhesive-backed polymer sheets cut

to the wafer diameter. Stresses induced in the wafer by the grinding and polishing processes must be controlled to prevent wafer and die warping. Wafer warping interferes with the die separation process (broken and cracked die). Die warping creates die-attach problems in the packaging process.[2]

Backside gold. Another optional wafer process is adding a layer of backside gold. A layer of gold is required on wafers that are going to be attached to the package by eutectic techniques (see the "Die attach" section). The gold is usually applied in the fabrication area (after backgrinding) by evaporation or sputtering.

Die separation

The chip-packaging process starts with the separation of the wafer into individual dies. The two methods of die separation are scribing and sawing (Fig. 18.15).

Scribing. *Scribing,* or *diamond scribing,* was the first production die-separation technique developed in the industry. It requires the alignment of the wafer on a precision stage, followed by dragging a diamond-tipped scribe through the center of the scribe lines. The scribe creates a shallow scratch in the wafer surface. The separation of the die is completed by stressing the wafer with a cylindrical roller. As the roller is moved over the surface, the wafer separates along the scribe lines. The breaks follow the crystal structure of the wafer, thus creating a right-angle edge on the die. Scribing becomes unreliable in wafers over 10 mils thick.

Sawing. The advent of thicker wafers has led to the development of sawing as the preferred die-separation method. A saw consists of a wafer table with rotation capability, a manual or automatic vision system for orienting the scribe lines, and a diamond-impregnated round saw. Two techniques are used. Both start with the passage of

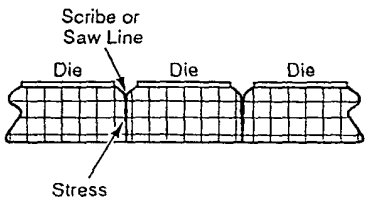

Figure 18.15 Scribe and saw separation.

the diamond saw over the scribe lines. For thinner wafers, the saw is lowered into the wafer surface to create a trench about one-third of the way through the wafer. The separation of the wafer into die is completed by the stress and roller technique used in the scribing method. The second sawing method is to separate the die by a complete saw-through of the wafer.

Often the wafers undergoing complete saw-through are first mounted on a flexible plastic film. The film holds the die in place after the sawing operation and aids the die-pick operation. Sawing is the preferred die-separation method due to the cleaner die edges and the fewer cracks and chips left on the sides of the die (Fig. 18.16).

Die pick and plate

After sawing, the separated die are transferred to a station for selection of the functioning die (nonlinked). In the manual method, an operator will pick up each of the nonlinked dies with a vacuum wand and place it in a sectioned plate. Wafers that come to the station on the flexible film are first placed on a frame that stretches the film. The stretching separates the die, which aids the die-pick operation.

In the automated version of this operation, a memory tape or disk with the locations of the good die (from wafer sort) is loaded into the tool. A vacuum wand picks up good die and automatically places them in a sectioned plate for transfer to the next operation.

Die inspection

Before being committed to the rest of the process, the die are given an optical inspection. Of primary interest is the quality of the die edge, which should be free of chips and cracks. This inspection also sorts out surface irregularities, such as scratches and contamination. Inspection may be manual with microscopes or automated with a vision system. At this step the die are ready to go into a package.

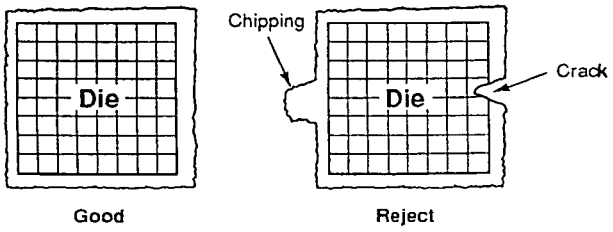

Figure 18.16 Die-separation results.

Die attach

Die attachment has several goals: to create a strong physical bond between the chip and the package, to provide either an electrical conducting or insulating contact between the die and the package, and to serve as a medium to transfer heat from the chip to the package.

A requirement is the permanency of the die-attachment bond. The bond should not loosen or deteriorate during subsequent processing steps or when the package is in use in an electronic product. This requirement is especially important for packages that will be subjected to high physical forces such as those used in rockets. Additionally, the die-attach materials should be contaminant-free and should not outgas during subsequent process heating steps. Lastly, the process itself should be productive and economical.

There are two principal methods of die attach, *eutectic* and *epoxy adhesives*.

Eutectic die attach. The eutectic method is named for the phenomenon that takes place when two materials melt together (alloy) at a much lower temperature than either of them separately. For die attach, the two eutectic materials are gold and silicon (Fig. 18.17). Gold melts at 1063°C, while silicon melts at 1415°C. When the two are mixed together, they start alloying at about 380°C. Gold is plated onto the die-attach area and alloys with the bottom of the silicon die when heated.

The gold for the die-attach layer is actually a sandwich. The bottom of the die-attach area is deposited or plated with a layer of gold. Sometimes a preformed piece of metal composed of a gold and silicon mixture is placed in the die-attach area. When heated, these two layers, along with a thin layer of silicon from the wafer back, forms a thin alloy layer. This layer is the actual bond forming the die-package attachment.

Eutectic die attach requires four actions. First is the heating of the package until the gold-silicon forms a liquid. Second is the placement

Conducting
- Gold/Silicon Eutectic
- Metal-Filled Epoxy
- Conducting Polyimide

Nonconducting
- Epoxy Adhesive
- Insulating Polyimide

Figure 18.17 Die-attach material matrix.

f the chip on the die-attach area. Third is an abrasive action, called scrubbing," that forces the die and package surfaces together. It is his action in the presence of the heat that forms the gold-silicon utectic layer. The fourth and final action is the cooling of the system, /hich completes the physical and electrical attachment of the chip nd package.

Eutectic die attach can be performed manually or by an automated nachine that performs the four actions. Gold-silicon eutectic die ttach is favored for high-reliability devices and circuits for its strong onds, heat dissipation properties, thermal stability, and lack of mpurities.

poxy die attach. The alternate die-attach process uses thick liquid poxy adhesives. These adhesives can form an insulating barrier etween the chip and package or become electrically and heat conlucting with the addition of metals such as gold or silver. Polyimide nay also be used as an adhesive. Popular adhesives are silver-filled poxy for copper lead frames and silver-filled polyimide for alloy 22 netal frames.[3]

The epoxy process starts with the deposit of the epoxy adhesive in he die-attach area by dispensing the adhesive with a needle or screen printing it into the die-attach area. The die, held by a vacuum wand, is positioned in the center of the die-attach area. The second action is to force the die into the epoxy to form a thin uniform layer nder the die. The final action is a curing step in an oven at an elevated temperature that sets the epoxy bond.

Epoxy die attach is favored for its economy and ease of processing, in that the package does not have to be heated on a stage. This factor makes the automation of the process easier. When compared to gold-silicon eutectic die attach, epoxy has the disadvantage of potential decomposition at the high temperatures of bonding and sealing operations. Epoxy die-attach films also do not have the bonding power of the eutectics.

Regardless of the attachment method used, there are several marks of a successful die attach. One is the proper and consistent alignment of the die in the die-attach area. Proper placement pays off in faster and higher-yield automatic bonding. Another desired result is a solid, uniform, and void-free contact over the entire area of the chip. This is necessary for mechanical strength and good thermal conduction. One evidence of a uniform bond is a continuous joint or "fillet" between the die edge and the package. The final mark of a good die-attach process is a die-attach area free of flakes or lumps that can come loose during use and cause a malfunction.

Bonding pad and package connection

Once the die and package are attached, they go to the bonding process. This is perhaps the most critical of all the assembly operations. Three techniques provide the critical chip to package connection:

- Wire bonding
- Flip-chip and bump
- TAB

The wire bonding procedure is simple in concept. A thin (0.7- to 1.0-mil) wire is first bonded to the chip bonding pad and spanned to the inner lead of the package lead frame. The third action is to bond the wire to the inner lead. Last, the wire is clipped and the entire process repeated at the next bonding pad. While simple in concept and procedure, wire bonding is critical because of the precise wire placement and electrical contact requirements. In addition to accurate placement, each and every wire must make good electrical contact at both ends, span between the pad and inner lead in a prescribed loop without kinks and be at a safe distance from neighboring wires. Wire loops in conventional packages are 8 to 12 mils, while those in ultrathin packages are 4 to 5 mils.[4] The distance between adjacent wires is called the pitch of the bonding.

Wire bonding is done with either gold or aluminum wires. Both are highly conductive and ductile enough to withstand deformation during the bonding steps and still remain strong and reliable. Each has its advantages and disadvantages and each is bonded by different methods.

Gold wire bonding. Gold has several pluses as a bonding wire material. It is the best-known room-temperature conductor and is an excellent heat conductor. It is resistant to oxidation and corrosion, which translates into an ability to be melted to form a strong bond with the aluminum bonding pads without oxidizing during the process. Two methods are used for gold bonding. They are *thermocompression* and *thermosonic.*

Thermocompression bonding (also known as *TC bonding*) starts with the positioning of the package on the bonding chuck and the heating of the chip and package to between 300 and 350°C. Chips that are going to be enclosed in an epoxy molded package are processed through die attach and bonded with the chip on the lead frame only. The bonding wire is fed out of a thin tube called a *capil-*

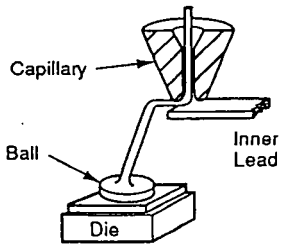

Figure 18.18 Gold ball bonding.

lary (Fig. 18.18). An instantaneous electrical spark or small hydrogen flame melts the tip of the wire into a ball and positions the wire over the first bonding pad. The capillary moves downward, forcing the melted ball onto the center of the bonding pad. The effect of the heat (thermal) and the downward pressure (compression) forms a strong alloy bond between the two materials. This type of bonding is often called *ball bonding*. After the ball bond is complete, the capillary feeds out more wire as it travels to the inner lead. At the inner lead, the capillary again travels downward to where the gold wire is forced by the heat and pressure to melt onto the gold-plated inner lead. The spark or flame then severs the wire, forming the ball for the next pad bond. This procedure is repeated until every pad and its corresponding inner pad are connected.

Thermosonic, gold ball bonding follows the same steps as thermocompression bonding. However, it can take place at a lower temperature. This benefit is provided by a pulse of ultrasonic energy that is sent through the capillary into the wire. This additional energy is sufficient to provide the heat and friction to form a strong alloy bond.

The majority of production gold wire bonding is done on automatic machines that use sophisticated techniques to locate the pads and span the wire to the correct inner lead. The fastest bonding machines can perform thousands of bonds per hour. There are two major drawbacks to the use of gold bonding wires. First is the expense of the gold. Second is an undesirable alloy that can form between the gold and aluminum. This alloy can severely reduce the conduction ability of the bond. It forms a purplish color and is known as the "purple plague."

Aluminum wire bonding. Aluminum wire, while not having the conduction and corrosion-resistance properties of gold, is still an important bonding wire material. A primary advantage is its lower cost. The second advantage is that the bond with the aluminum bonding pad is a monometal system and thus less susceptible to corrosion. Also, aluminum bonding can take place at lower temperatures than gold bonding, making it more compatible with the use of epoxy die-attach adhesives.

The bonding of the aluminum follows the same major steps as gold wire bonding. However, the method of forming the bond is different. No ball is formed. Instead, after the aluminum wire is positioned over the bonding pad, a wedge (Fig. 18.19) forces the wire onto the pad as a pulse of ultrasonic energy is sent down the wedge to form the bond. After the bond is formed, the wire is spanned to the inner lead where another ultrasonic-assisted wedge bond is formed. This type of bonding is known variously as *ultrasonic* or *wedge bonding*.

After this bond, the wire is cut. At this point in the process, a major difference between the bonding of the two materials occurs. In gold bonding, the capillary moves freely from pad to inner lead, to pad, and so on, with the package in a fixed position. In aluminum wire bonding, the package must be repositioned for every single bonding step. The repositioning is necessary to line up the pad and inner lead along the direction of travel of the wedge and wire. This requirement places an additional difficulty on the designers of automatic aluminum bonding machines. Nevertheless, most production aluminum bonding is done on high-speed machines.

Flip-chip and bump technology

Wire bonding presents several problems. Minimum height limits are imposed by the required wire loops. There is a chance of electrical performance problems or shorting if the wires come too close to each other. The wire bonds require two bonds and must be placed one-by-one and there are resistances associated with each bond. These problems are addressed by replacing wires with a deposited metal *bump*

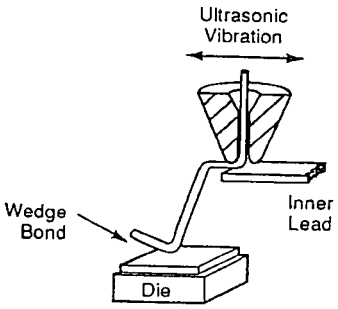

Figure 18.19 Aluminum wedge bonding.

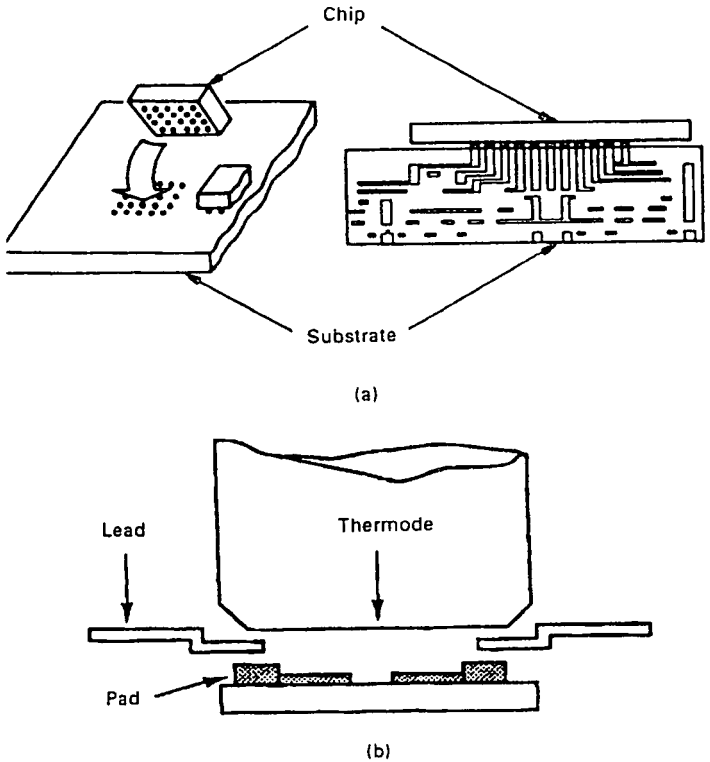

Figure 18.20 (*a*) Flip-chip joining; (*b*) tape automatic bonding. (*Source: Microelectronics Packaging Handbook by Tummala and Rymaszewski*)

on each bonding pad. Connection to the package is made when the chip is flipped over and soldered. Each bump connects to a corresponding package inner lead (Fig. 18.20*a*). Packages are lower profile, the electrical connection has lower resistance, and the electrical path is much shorter. IBM calls its version of this technology *controlled collapse chip connection* (C4).[5]

Tape automated bonding. Tape automated bonding (TAB) is used to wire up chips when extreme package thinness is required, such as in credit-card-size radios. The TAB process starts with formation of the lead system on a flexible strip of tape. Various methods are used to form the lead system. The metal for the system is deposited on the tape by sputtering or evaporation. Formation of the lead system is either by mechanical stamping or patterning techniques similar to the fabrication patterning process. The result is a continuous tape

containing many individual lead systems. For the bonding operation (Fig. 18.20*b*), the chip is positioned on a chuck and the tape is moved by sprockets until one of these lead systems is positioned exactly over the chip. In this position, the inner leads of the system should be positioned over the bonding pads of the chip.

The bond is completed with a tool known as a *thermode.* The thermode is faced with a flat diamond surface and is heated. The thermode is moved downward, first contacting the inner leads. It continues downward with enough pressure to force the inner leads onto the bonding pads. The heat and the pressure are regulated to cause a physical and electrical bond between the two. Large chips require a larger TAB bonding area. For these chips, the thermode is faced with a synthetic diamond.

TAB bonding is also used in conjunction with package bonding. The advantages of TAB are speed, in that all of the bonds to the chip are made in one action, and the ease of automation offered by the tape and sprocket system.

Preseal inspection

An important step in the chip-packaging process is the preseal or precap inspection, sometimes called *third optical inspection,* which takes place after the bonding step. The inspection is performed to provide feedback on the quality of the operations already performed. It also is performed to reject packaged chips that may represent reliability hazards when the chip is in operation in the field.

While there are many levels of inspection criteria, they fall into two main categories: commercial and high-reliability (hi-rel). The commercial inspections are given to chips and packages destined for use in commercial systems and are derived from the internal quality levels of the producing company in conjunction with its experience and customer specifications. The high-reliability specifications are derived from a set of government standards called "Mil-Standard 883."

Commercial-level inspections screen the bonded chips for die-attach quality; correct placement of the bonds on the bonding pads and inner leads; the shape and quality of the ball or wedge bond; and the general condition of the chip surface in regard to contamination, scratches, and the like.

Mil-Standard 883 covers the same general issues as the commercial inspections, but to more stringent requirements. In particular, this standard also specifies criteria for the chip surface, including pattern alignment, critical dimensions, and surface irregularities, such as small scratches, voids, and small defects. These criteria serve to reject

bonded chips that may malfunction in the rigorous conditions encountered in space and military operation.

Sealing techniques

After the bonded chip passes the optical inspection, it is ready for sealing in a protective enclosure. There are several methods used to achieve the enclosure of the chip. The method chosen depends on whether the seal must be hermetic or nonhermetic, and which type of package is to be used. The principal sealing methods use welded seals, soldered seals, glass-sealed lids, CERDIP package construction, and molded epoxy enclosures (Fig. 18.21).

Metal can. If the package is a metal can type, a hermetic seal is achieved by welding the flanged lid to a matching flange on the base of the package.

Premade packages. Premade ceramic packages are sealed by one of two methods, metal or ceramic lids (Fig. 18.22). Packages made for metal lids have a ring of gold around the top of the die-attach cavity, called the *seal ring*. Placed on top of the seal ring area is a preformed piece of gold-tin solder. The metal lid is clamped in position over the seal ring and placed on the belt of a conveyor furnace. As the clamped package passes through the furnace, the lid and package are soldered

Hermetic
- Welding
- Soldered Lid
- Glass-Sealed Lid or Top

Nonhermetic
- Epoxy Molding
- Blob Top

Figure 18.21 Package sealing methods.

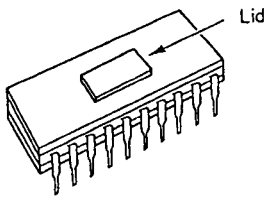

Figure 18.22 Premade ceramic package.

together to form a hermetic seal. The sealing takes place at a temperature range of 320 to 360°C in a pure nitrogen atmosphere.

If the package is to receive a ceramic lid, the procedure is similar. The part of the ceramic lid that contacts the base, outside the die-attach area, is coated with a layer of low-melting-point glass. The hermetic seal is completed as the package passes through a conveyor furnace. This sealing takes place at a temperature of about 400°C in an atmosphere of clean dry air.

CERDIP packages. A completed CERDIP package results in a hermetic seal around the chip and bonding wires. This seal is accomplished with glass, similar to the ceramic seal on the premade packages. In the case of the CERDIP package, the inner metal lead system is buried in a glass layer. The ceramic top of the package system has a cavity (Fig. 18.23). The underside of the lid, outside the cavity area, is coated with a layer of low-melting-point glass. The lid is placed over the base and clamped. The seal is accomplished as the assembly is passed through a conveyor furnace or placed in an oven. In the furnace or oven, the glass melts, fusing the base and top together. The CERDIP glass sealing system is used to seal DIP and flat packs. These latter packages are known as *Cerpacks* and *Cerflats*.

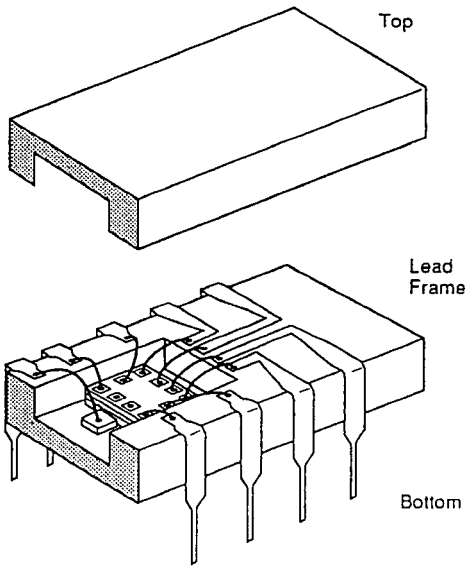

Figure 18.23 CERDIP parts.

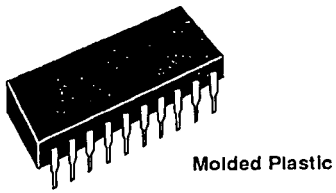

Figure 18.24 Molded CERDIP.

Molded epoxy enclosures. The fourth major method of enclosure, *epoxy molding,* produces the plastic package (Fig. 18.24). The resultant seal, while protecting the die from moisture and contamination, is not classified as hermetic. However, there exists a considerable amount of research into the development of improved epoxy materials to create better enclosures. The major advantages of epoxy molded enclosures are weight, low material cost, and manufacturing efficiency.

This sealing method follows a different process flow. The die is attached and bonded to a lead frame containing a number of lead systems (Fig. 18.25). After the preseal inspection, the lead frames are transferred to the molding area. The frames are placed on a mold mounted in a transfer molding machine. The molding machine is in turn charged with pellets of the epoxy material, which have been previously softened by a radio-frequency heater. Inside, the pellets are forced by a ram into a liquid state. The ram then forces the liquid around the die on the lead frames, forming an individual package

Figure 18.25 Lead frame.

around each lead frame. After the epoxy sets in the mold, the frames are removed and placed in an oven for final curing.

Lead plating

An important feature of the completed package is the finish on the package leads. Most package leads are coated with lead-tin solder, tin plate, or gold plate. The plating serves several important functions. First is the solderability of the leads into a circuit board. The additional metal finish improves the lead solderability, resulting in a more reliable electrical connection of the package and the printed circuit. The second benefit of the lead finish is that it protects the leads from oxidation or corrosion during periods of storage prior to mounting on the circuit board. The third benefit of lead plating is the protection of the leads from corrosive agents in the packaging and printed-circuit board mounting processes. These agents include solder flux, corrosive cleaners, and even tap water. The plating continues to protect the leads during their lifetime of use.

Electrolytic plating. Plated layers, such as gold and tin, are applied by electrolytic procedures. The packages are mounted on racks with each lead connected to an electric potential. The racks are placed in a tank containing a plating solution. Next, a small current is passed between the packages and an electrode in the tank. The current causes the particular metal in the solution to plate onto the leads.

Tin-lead solder. Tin-lead solder layers are applied either by dipping the packages into a pot of the molten solder or by a wave soldering technique. This latter technique offers the advantage of good control of the layer thickness and provides a shorter exposure of the package to the molten solder.

Plating process flows

Metal cans, side-brazed DIP packs, and pin grid arrays have their leads plated before starting into the packaging process. CERDIP and plastic packages go through the plating process after the sealing steps.

Lead trimming

One of the last steps in the package assembly process is trimming away excess material from the leads. The outer leads of DIP and flat-pack packages are made with a tie-bar (Fig. 18.26). This bar keeps the leads from becoming bent during the packaging process. At the

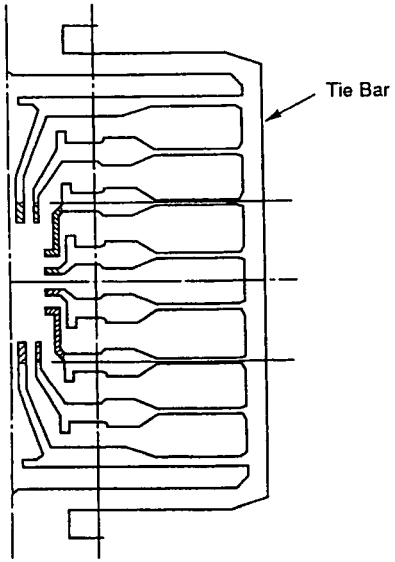

Figure 18.26 Tie-bar.

end of the process, the package goes through a simple trimming machine that simultaneously trims away the tie-bar and trims the leads to the proper length.

Plastic package lead frames have an additional piece of material. It is a bridge of metal close to the package body that functions as a dam to prevent the liquid epoxy material from running into the lead area (Fig. 18.27). The dam is cut away from the frame with a series of precise cutting tools. After the dam is cut away, the packages move to another station on the cutter where the frame is separated into individual packages. If the package is a surface-mount type, the leads will be bent into the required shape.

Deflashing

Plastic packages receive an additional process, called *deflashing,* which is required to remove excess molding material from the package enclosure. Deflashing is done by either dipping the packages in a chemical bath followed by a rinse or by a physical abrasion process. Physical deflashing is done in a machine similar to a sand blaster which uses plastic beads as the abrasive.

Package marking

Once completed, a package must be identified with key information. Typical information coded on the package is the product type, device

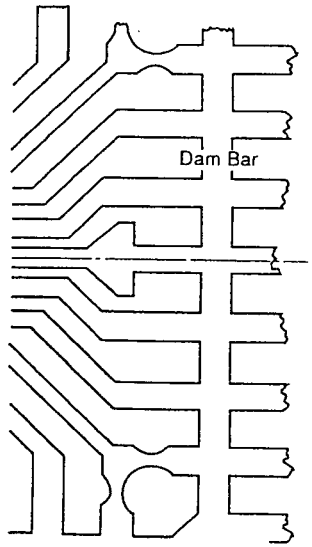

Figure 18.27 Lead frame dam.

specifications, date, lot number, and where it was made. The main methods of marking are ink printing and laser inscription. Ink printing has the advantage of good adherence to all of the package materials. The composition of the ink is chosen for permanence in the eventual operating environment of the device. The ink is applied by an offset printer followed by a curing step. Curing is done by oven drying, room temperature air drying, or by ultraviolet light.

Laser printing is especially suited for plastic packages. The mark is permanently inscribed in the package surface and can provide good contrast on the dark packages. Additionally, laser marking is fast and noncontaminating since no foreign material is added to the package surface and no curing step is required. A drawback to laser marking is the difficulty of changing the mark if a wrong code was used or the status of the device is changed. Regardless of the marking method, all marks must meet the requirements of legibility, especially on smaller packages, and permanence when exposed to harsh environments.

Final testing

At the conclusion of the packaging process, the completed package is put through a series of environmental, electrical, and reliability tests. These tests vary in type and specifications, depending on the customer and use of the packaged devices. The tests may be performed on all of the packages in a lot or on selected samples.

Environmental tests

Environmental tests are performed to weed out leaking and defective packages. Defects detected are loose chips, contaminants and particles in the die-attach cavity, and faulty bonding. This testing series starts with a stabilization bake to drive off any volatile substances in the package. A typical bake is at 150°C for 24 hours.

The first environmental test is *temperature cycling*. The packages are loaded into a chamber and cycled between two temperature extremes. The number of cycles may reach several hundred. The high and low temperatures of this test vary with the device use. Commercial parts receive a narrower temperature range than hi-rel parts. The hi-rel cycle range is −25 to 125°C. During the cycling any weakness in the seal, die attachment, or bonding will be aggravated and be detected in later electrical tests.

A second environmental test is *constant acceleration*. In this test the packages are accelerated in a centrifuge (Fig. 18.28) that creates a force as high as 30,000 times the pull of gravity on the earth (30,000 g). During the acceleration, loose particles in the package, poorly attached dies, and weakly attached bonds are stressed so that they will be detected at the final electrical tests.

Leaks in the package enclosure are detected by two tests. *Gross leak* testing (Fig. 18.29) is conducted by submerging the packages in a hot liquid. The heated liquid raises the temperature of the package and forces trapped gases in the cavity to escape. The escaping gases are observable as bubbles rising in the liquid. The chamber has a transparent side, allowing an operator to observe the bubbles. Smaller (or fine) leaks are detected by using tracer gases. For this check, helium is pumped under pressure into a chamber containing the packages. If the package has small leaks, the gas will be pumped into the package cavity. The gas is detected as it escapes through the small leaks by a machine known as a mass spectrometer, which can

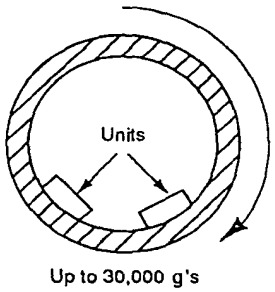

Figure 18.28 Acceleration test.

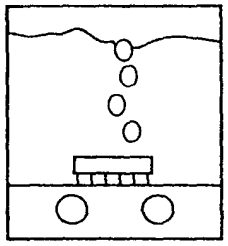

Figure 18.29 Gross leak bubbles test.

identify the escaping gas. An alternate fine leak test uses the radioactive gas krypton-85. It too is pumped through any leaks into the package under pressure. Detection of any krypton-85 in the package is by a device similar to a Geiger counter.

Electrical testing

The purpose of the wafer-fabrication and packaging processes is to provide to the customer a specific semiconductor device that performs to specific parameters. Thus, one of the last steps is an electrical test of the completed unit to verify that it performs to the specifications. The tests are similar to the wafer-sort tests. The overall objective is to verify that the good chips identified at wafer sort have not been compromised by the packaging process.

First there is a series of parametric tests. These electrical tests check the general performance of the device or circuit and ensure that it meets certain input and output voltage, capacitance, and current specifications. The second part of the final test is called the *functional test*. This test actually exercises; the specific chip functioning. Logic chips are put through logic tests; memory chips are exercised in their data storage and retrieval capabilities.

The equipment used to conduct the final test is electrically similar to that used in the wafer-sort operation. The electrical tests are performed by a computer-controlled tester that directs the sequences and levels of the parametric and functional tests. The packages are connected to the tester through sockets; the socket unit is known as the *test head*. The packages are inserted into the test head manually or by an automatic unit known as a *handler* (Fig. 18.30). This handler may be mechanical or robotic, depending on the speed and complexity of the operation.

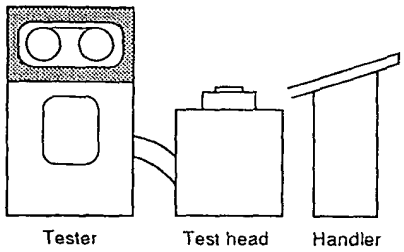

Figure 18.30 Final test.

Burn-in tests

The last of the tests is the optional burn-in test(s). The reason it is optional is that although it is required for all high-reliability device lots, it may or may not be performed on commercial devices. The test requires the insertion of the packages in sockets and mounting in a chamber with temperature-cycling capability. During the test, the circuits are temperature-cycled while under an electrical bias.

The burn-in test is intended to stress the electrical interconnection of the chip and package and drive any contaminants in the body of the chip into the active circuitry, thus causing failure. This test is based on data that indicate that chips prone to these types of failures actually malfunction in the early part of their lifetime. By conducting burn-in tests, the early failures are detected. The devices passing the test are statistically more reliable.

Package Process Flows

It should be obvious that there is no universal packaging process flow. The package construction technique and lead-plating requirements dictate the flow. The table in Fig. 18.31 illustrates typical flows for three of the more common package types.

Packaging Strategies

Integrating a chip into an electronic product or system requires an electrical subsystem between the chip and the system. Two main approaches have emerged, individual packaging and bare die techniques (Fig. 18.32).

Individual package

With individual packaging, there are three techniques used to connect the package to a printed-circuit board (PCB). They are through-

Process Step	Premade Ceramic	CERDIP	Epoxy Molded
Die Separation	X	X	X
Pick and Plate	X	X	X
Die Attach	X	X	X
Wire Bonding	X	X	X
Preseal Inspect	X	X	X
Lid Sealing	X	X	
Epoxy Molding	X		
Deflashing	X		
Lead Plating and Trim		X	X
Marking	X	X	X
Environmental Test	X	X	X
Final Electric Test	X	X	X
Burn-In	X	X	X

Figure 18.31 Table of packaging process flows.

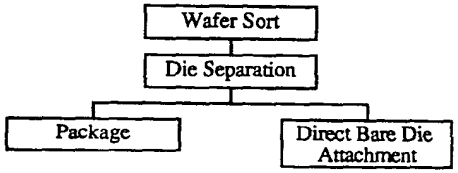

Figure 18.32 Post die-separation options.

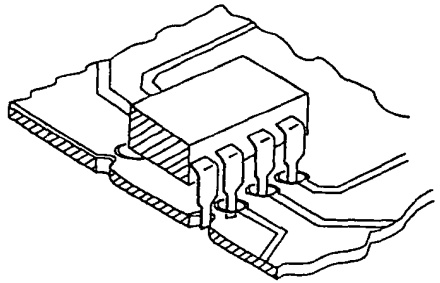

Figure 18.33 Dip through-hole assembly.

hole, surface mount, and TAB. Through-hole connections feature straight pins on the package, which are inserted into corresponding holes in the printed-circuit board. (Fig. 18.33). A newer method is *surface mount,* also referred to as *SMD.* This method features packages that have their leads bent into a J shape or bent outward to allow direct soldering to the board surface (Fig. 18.34).

Some SMD packages do not have leads—instead, they terminate in metal traces hugging the package body. They are known as *leadless*

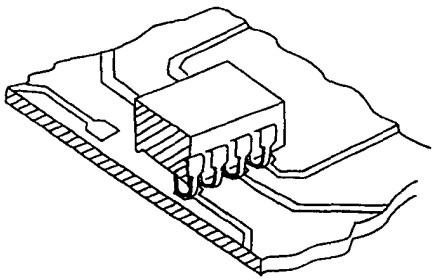

Figure 18.34 Surface-mount device.

packs. For inclusion on a circuit board, they are inserted into chip carriers, which in turn have leads that attach to the printed-circuit board.

Tape automated bonding (TAB) has two uses. One is bonding the chip bonding pads directly to the lead frame (See section on bonding). TAB is also a technique for bonding the outer leads directly to the PCB.

Bare die techniqu s

More reliable, higher-density, and faster circuits are an ongoing goal and challenge. Reliability is addressed in hybrid circuits. Speed and higher density comes with the elimination of the individual die package. Fewer links in the chain reduce resistances and (in some cases) shorten the length carriers have to travel, hence increasing speed. This strategy, called bare die, is used in hybrid circuits, multichip modules, and chip-on-board technology.

Package Design

Up to the early 1970s, most chips ended up in either a metal package, known as a "can," or in the familiar dual in-line package (DIP). The trends in chip size and integration levels and new electronic products with special packaging requirements (smart cards) have driven the development of new packages and strategies.

Metal cans

Metal cans are cylindrically shaped packages with an array of leads extending through the base (see Fig. 18.35*a*). The chip is attached to the base and wire-bonded to posts that are connected to the leads. The lid and base have matching flanges that are welded together to

create a hermetic seal. These packages are designated by numbers, with the T0-3 and T0-5 being the most common. Metal cans are used to package discrete devices and small-scale integrated circuits.

Dual in-line packages (DIPs)

The DIP is probably the most familiar package design. It features a thick, sturdy body with two rows of outer leads coming out of the side and bending downward. DIPs are constructed by three different techniques (Fig. 18.35*b*). Chips designed for high-reliability use will be packaged in a premade ceramic DIP. The package is formed with a solid body of ceramic with the leads buried in the ceramic. The die-attachment area is a cavity recessed into the body. The hermetic seal is completed by a soldered metal lid or a glass-sealed ceramic lid.

Another approach to the DIP is the CERDIP, which stands for ceramic DIP. This type of package is composed of a bottom ceramic base with the lead frame held firm in a glass layer. The chip is attached to the base and wire-bonded to the lead frame. The hermetic seal is completed with a ceramic top glass sealed to the base. CERDIP

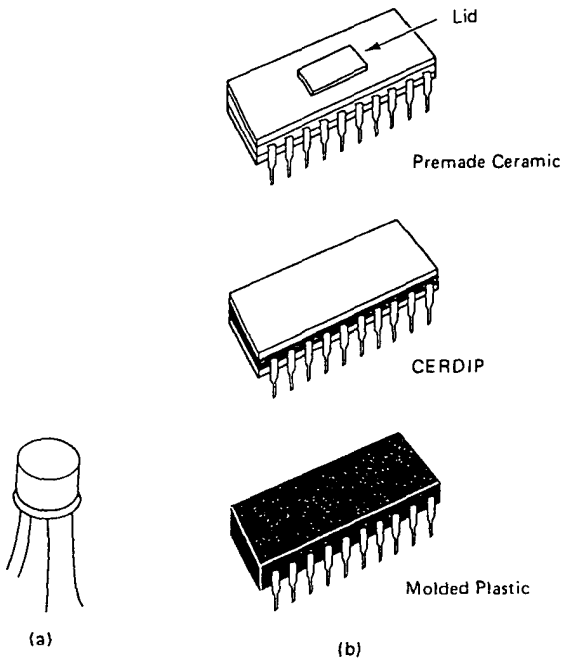

Figure 18.35 (*a*) Metal can; (*b*) DIP packages.

ruction is used for a number of package types. The vast majority Ps are made by the epoxy molding technique. In this technique hip is attached to a lead frame and then wire-bonded. After ıng the frame is placed in a molding machine and the package is ɔd around the chip, wire bonds, and inner leads.

ɾid arrays

ɜr chips, with more leads, have outgrown the DIP configuration. ɔin grid array (PGA) is a package designed for larger chips. It res a premade "sandwich" with the outer leads coming out of the m of the package in the form of pins (Fig. 18.36). The chip is hed in a cavity that is formed in either the top or bottom of the Connections to the chip cover the entire chip area (unlike most , which have connections restricted to bonding pads around the hery of the chip). Ceramic PGAs are hermetically sealed with a red metal lid.

rid arrays (BGAs)

ɜ have the same body shape as PGAs. Instead of pins on the ıge bottom, there is a series of solder bumps (balls) used to con- the package to the PCB (see "Flip-chip and bump technology"). ɜffect is to lower the package profile and weight as well as pro- higher pin counts by using the whole chip surface for bonding

packages

ɜ pin grid array packs are a convenient design for larger chips, ceramic construction is expensive compared to molded epoxy ıges. This consideration led to the development of the quad pack- A quad (short for quadrant) pack is constructed by the epoxy-

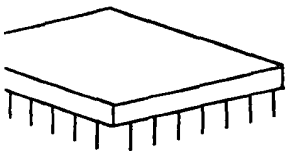

Figure 18.36 Pin grid array.

molded technique but has leads coming out of all four sides of the package (Fig. 18.37).

Thin packages

New products such as smart cards require thin packages. There are several techniques used to make thinner packages. They are called flat packs (FPs), thin small outline packages (TSOPs), small outline IC (SOIC), and ultrathin packages (UTPs). Flat packs are constructed by the same techniques used to form DIP packages. These packages are designed with flatter height profiles and have leads bent out to the side of the package (Fig. 18.38). Ultrathin packages have total body heights in the 1-mm range. There are also quad flat packs (QFPs).

Lead on chip (LOC)

The LOC package, intended for large die, have the bonding pads arranged down the middle of the chip (Fig. 18.39). Package leads sit on a cushion over the chip surface.

Hybrid circuits

Hybrid circuitry is an old technology long favored for use in military and harsh environments. Hybrid circuits consist of a substrate on which standard electrical and semiconductor devices are mounted. The devices are connected by conductive or resistive thick-film paths

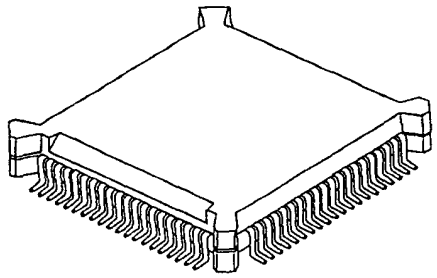

Figure 18.37 Quad package.

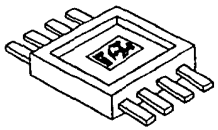

Figure 18.38 Flat pack.

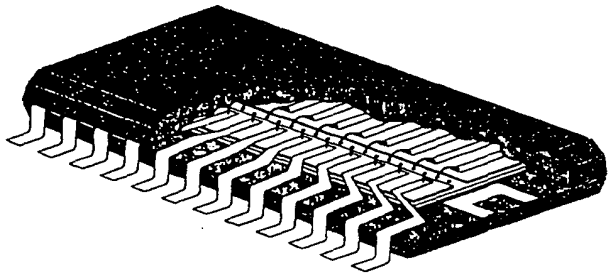

Figure 18.39 Lead on chip (LOC). (*Source: Semiconductor International, May 1993*).

on the surface of an insulating substrate. These paths are formed by silk-screening inks containing a proper filler or from thin films evaporated or sputtered onto the surface and patterned by photolithography techniques. The term *hybrid* refers to the mix of solid-state and conventional passive electrical devices (resistors, capacitors) present in the same circuit. Most hybrid substrates are ceramic. High-performance hybrids may have aluminum nitride (AlN), silicon carbide (SiC), or diamond substrates used alone or in combinations.[6]

Hybrid circuits offer the advantages of structural rigidity and low leakage between devices due to the insulating property of the ceramic. They can provide a circuit with a mix of CMOS, bipolar, and other components and offer functions not available in ASIC circuits.[7]

On the downside, they generally have a much lower density than integrated circuits at a higher cost.

Multichip modules (MCMs)

Mounting individual chip packages on a PCB presents several problems. A chip package is several times the area of the chip, and so takes up space on the board. Circuit resistance is increased by the individual resistances of all the package pins, and the electrical path lengths are multiplied by the number of chips and package leads. Each of these problems can be reduced by mounting several chips on the same substrate. This technology, multichip module (MCM), is similar to that used by hybrid circuits, but thick-film screened components are rarely used.

Three types of MCMs have evolved. MCM-L (laminated) is similar to advanced, laminated printed-circuit boards, using copper foil conductors on plastic dielectrics. MCM-C (ceramic) are more like hybrid circuits. The substrate is a cofired ceramic with thick-film conductors. MCM-D (deposited) uses ceramic, metal, or silicon substrates with deposited thin metal conductors.

Chip on board (COB)

The most direct use of bare die is to bond them directly to the printed-circuit board. Bonding techniques include all those used to bond chips into packages. After connection, the chip is protected by a technique called *blob top protection.* The protection is accomplished by covering the chip and bonds with a blob of epoxy resin material (Fig. 18.40). The material is similar in properties to that used to mold the plastic packages. Blob top coverings are used with TAB and other packaging schemes.

The known good die (KGD) problem

In the individual package process, a final test assures quality of the completed product. If the chip had gone bad or the process was faulty, the entire chip and package is discarded. But the cost is much higher when putting bare die into hybrid, MCM, and printed-circuit boards. These vehicles are more expensive to build and carry other expensive chips or components.

One option is to rely on the results of the wafer-sort test to certify die performance. Unfortunately, wafer sort does not include environmental tests or long-term reliability tests. However, performing a final test on a bare die is difficult, if not impossible. Consequently, before the bare-die step, some temporary assembly of the die to a lead frame must be done to facilitate a full final test.

Summary

There are thousands of individual package types and there is no uniform system of identifying them. Some are named by their design (DIP, flat packs, etc.), some are named by their construction technique (molded, CERDIP, etc.), and others are named by their use (e.g.,

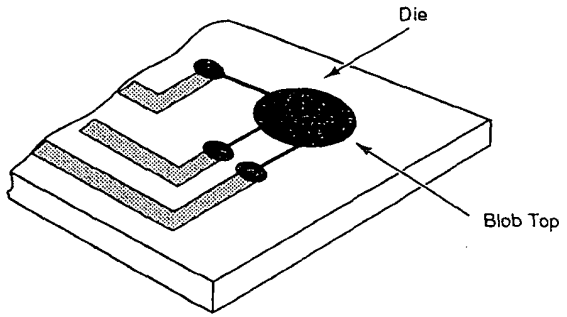

Figure 18.40 Blob top.

SMDs). When trying to understand a package type, keep in mind the three considerations: design type, construction technique, and use.

Key Concepts and Terms

Bare die strategies
Bonding
Cleanliness requirements
Die attach
Final test(s)
Hermetic and nonhermetic seals
Package designs
Package functions
Package parts
Pick and plate
Sealing techniques

Review Questions

1. Name the four functions of a chip package.
2. What is the function of marking dies with ink dots?
3. Name the five parts of a package.
4. Define a hermetic package.
5. Give an example of a hermetic and nonhermetic package.
6. List in order the six major steps in the packaging process.
7. Describe the process and material used for eutectic die attachment.
8. Describe the principal thermosonic and ultrasonic bonding techniques.
9. What is a DIP package and how is it formed?
10. Name two methods of package marking.

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Glossary

acceptor An impurity that causes semiconducting materials to accept valence electrons, thereby leaving "holes" in the valence band. The holes act like carriers of positive charge, referred to as P type.

aligner (align and expose) A process tool used to align wafers and masks or reticles and expose the photoresist with a UV or other radiation source.

alignment Refers to the positioning of a mask or reticle with respect to the wafer.

alignment marks Targets on the mask and wafer used for correct alignment.

alloy (1) A compound composed of two metals. (2) In semiconductor processing, the alloy step causes the interdiffusion of the semiconductor and the material on top of it, forming on ohmic contact between them.

aluminum (Al) The metal most often used in semiconductor technology to form the interconnects between devices on a chip. It can be applied by evaporation or sputtering.

amorphous Materials with no definite arrangement of atoms, e.g., plastics are amorphous.

angstrom A unit of length, an angstrom (Å) is one ten-thousandth of a micron (10^{-4} μm) or 100,000,000 Å = 1 cm.

anistropic An etch process that exhibits little or no undercutting.

anneal A high-temperature processing step (usually the last one), designed to minimize stress in the crystal structure of the wafer.

antimony (Sb) A Group V element that is an N-type dopant in silicon. It is often used as the dopant for the buried layer.

Source: Glossary terms are abstracted from Beverly Griggs, Anne Miller, and Peter Van Zant, *Semiconductor Terminology—Graphic Glossary of Terms,* Semiconductor Services, Redwood City, Calif., 1989.